

CLAIMS

What is claimed is:

1. A bus device adapted to be coupled to a bus, comprising:
a clock generator that is adapted to generate a clock signal for internal use by the bus device;
data synchronizing logic that is adapted to synchronize source synchronous data that the bus device receives from the bus to the bus device's clock signal; and
error detection and correction logic coupled to the data synchronizing logic, the error detection and correction logic is adapted to detect and correct errors associated with the data received from the bus concurrently while the data synchronizing logic synchronizes source synchronous data received from the bus to the clock signal.
2. The bus device of claim 1 further comprising a selection device coupled to the data synchronizing logic, the bus, and the error detection and correction logic, wherein the selection device selectively provides to the error detection and correction logic synchronized data from the data synchronizing logic or common clocked data from the bus that has not been synchronized by the data synchronizing logic.
3. The bus device of claim 1 further comprising a megacell coupled to the bus and to the error detection and correction logic, wherein said megacell arbitrates for control of the bus and receives corrected data from the error detection and correction logic.
4. The bus device of claim 3 wherein the error detection and correction logic computes expected error correction code bits for common clocked data and provides the computed expected error correction code bits to the megacell for correction of bit errors, if any.

5. The bus device of claim 3 further comprising a multiplexer coupled to the data synchronizing logic, the bus, and the error detection and correction logic, wherein the multiplexer provides either synchronized data from the data synchronizing logic or common clock data from the bus to the error detection and correction logic as dictated by a control signal from the megacell.

6. Thus bus device of claim 1 wherein data synchronizing logic receives a plurality of source synchronous data units from the bus, each data unit received in a separate cycle of a clock transmitted with each source synchronous data unit, and each data unit is provided to the error detection and correction logic which detects errors in each data unit while the data synchronizing logic receives and synchronizes a subsequent source synchronous data unit.

7. A system comprising:
a plurality of devices;
a bus coupling together the plurality of devices, wherein source synchronous and common clocked data transactions can occur over the bus between the devices;
wherein each device comprises a megacell coupled to a synchronization and error detection/correction module, the megacell implementing a protocol associated with the bus and the synchronization and error detection/correction module synchronizing source synchronous data while concurrently detecting errors with such source synchronous data.

8. The system of claim 7 wherein each device comprises a clock generator that is adapted to generate a clock signal for internal use by the device and each synchronization and error detection/correction module comprises:
data synchronizing logic that is adapted to synchronize source synchronous data that the device receives from the bus to the bus device's clock signal; and

error detection and correction logic coupled to the data synchronizing logic, the error detection and correction logic is adapted to detect and correct errors associated with the data received from the bus concurrently while the data synchronizing logic synchronizes source synchronous data received from the bus to the clock signal.

9. The system of claim 7 wherein a device receives a plurality of source synchronous data packets and detects an error in each data packet while receiving and synchronizing a subsequent data packet.

10. The system of claim 7 wherein each synchronization and error detection/correction module receives source synchronous data and common clocked data and the synchronization and error detection/correction module detects and corrects errors for source synchronous data before providing such data to the megacell, but generates expected ECC bits for common clocked data without correcting errors associated with said common clocked data.

11. A bus device adapted to be coupled to a bus, comprising:
a clock generator that is adapted to generate an clock signal for internal use by the bus device; and
means for receiving source synchronous data from the bus and for synchronizing the source synchronous data to the clock while simultaneously detecting errors associated with the source synchronous data.

12. The bus device of claim 11 further comprising means for detecting and correcting errors associated with the source synchronous data simultaneously while synchronizing the source synchronous data.

13. The bus device of claim 11 further comprising means for receiving common clocked data and for detecting and correcting errors associated with

the source synchronous data and for generating ECC bits without correcting errors associated with common clocked data.

14. A bus device adapted to be coupled to a bus, comprising:
 - a clock generator that is adapted to generate a clock signal for internal use by the bus device;
 - data synchronizing logic that is adapted to synchronize source synchronous data that the bus device receives from the bus to the bus device's clock signal; and
 - error detection and correction logic coupled to the data synchronizing logic, the error detection and correction logic is adapted to detect and correct errors associated with the data received from the bus within a time period allocated to the data synchronizing logic to synchronize source synchronous data.
15. The bus device of claim 14 wherein the error detection and correction logic comprises a plurality of ECC generation and correction logic units and at least one, but not all, of the ECC generation and correction logic units also comprises parity logic.
16. The bus device of claim 15 wherein only one of the ECC generation and correction logic units comprises parity logic.
17. A method usable in a device having an internal clock and capable of receiving an external clock, the internal clock having a frequency that is different from that of the external clock, the method comprising:
 - receiving a plurality of source synchronous data portions in separate cycles of the external clock; and
 - synchronizing the received data portions to the internal clock while concurrently detecting and correcting errors in the received data portions.

18. The method of claim 17 further comprising correcting errors in the received data portions concurrently with receiving a data portion and making the timing associated with the data portion comport with the timing of the internal clock.

19. The method of claim 17 further receiving a common clocked data, detecting and correcting errors of source synchronous data, and detecting, but not correcting, errors of common clocked data.